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Development of a 50 A Nanosecond Current Step Generator for High-Bandwidth Current Sensor Characterisation

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24GRD05 ELITE | WP4 | FFII - LCOE

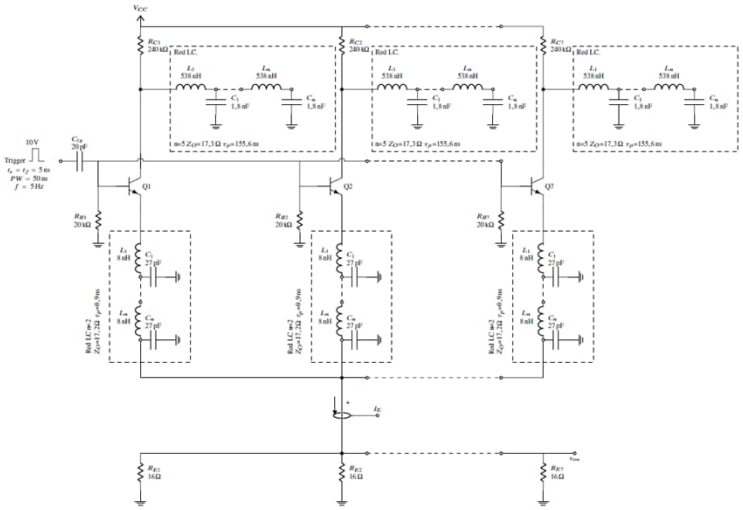
FFII experimentally validated the modular generator building block and defined a seven-branch design for operation up to 50 A.

1 ELITE WP4 Task 4.2 NEED

The objective of this task is to characterize high bandwidth current sensors with step response measurements. The current step generator must deliver short current steps with nanosecond rise times up to 50 A.

2 GENERATOR ARCHITECTURE WITH AVALANCHE TRANSISTORS

Seven matched branches in parallel. Each uses an FMMT417TD avalanche transistor, its own LC pulse-forming network and a 16 Ω emitter resistor to limit the current. Additional LC networks are connected in series to synchronise switching among transistors.



Seven matched avalanche-transistor branches switch together to scale current.

LC network ≈17.3 Ω Duration ≈155.6 ns

300 V supply ⟶ 51.5 A calculated

3 OPERATING PRINCIPLE

DC supply › **LC pulse-forming networks** › **Avalanche switches** › **Parallel current addition** › **Sensor under test**

The DC supply charges each LC network. The avalanche switches enter second breakdown almost simultaneously. The seven branch currents add at the sensor under test.

4 EXPERIMENTAL VALIDATION

VALIDATED PROTOTYPE

2 parallel branches. 16-stage LC networks (≈12 Ω). Mean pulse: 19.3 A measured. Rise time: 10.1 ns measured. LC section count controls pulse width.

FINAL 50 A DESIGN

7 branches with 16 Ω emitter resistors and ≈17.3 Ω LC networks. Calculated current: 44.6–51.5 A. Target pulse width: ≈300 ns. Matched LC networks replace RG-174 timing cables.

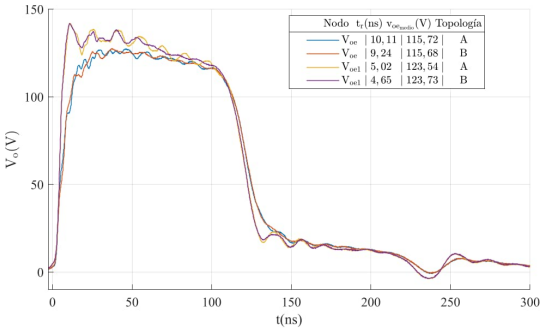
19.3 A

PROTOTYPE · MEASURED (ONLY TWO BRANCHES)

↓ SCALING METHODOLOGY

44.6–51.5 A

FINAL DESIGN · CALCULATED



5 DESIGN PARAMETERS

Parameter	Validated prototype	Final architecture
Parallel branches	2	7
Current	19.3 A measured	44.6–51.5 A calculated
Emitter resistance	12 Ω per branch	16 Ω per branch
LC impedance	12.0 Ω	17.3 Ω
Synchronisation	RG-174 cable	Matched LC network
Switch	FMMT417TD	FMMT417TD

The 19.3 A prototype result is measured. The final 44.6–51.5 A range and ≈300 ns width are design targets pending verification.

6 KEY DESIGN FINDINGS

Parallel: Matched branches add current without Marx.

Matching: LC impedance ≈10–15% above emitter resistance compensates transistor resistance and reduces reflections.

LC networks: Set pulse width and replace long coaxial timing lines.

Parasitics: Lower inductor series resistance flattens the pulse.

7 NEXT STEPS IN ELITE WP4

01 Fabricate the seven-branch PCB
02 Measure the full range up to 50 A
03 Test repeatability and thermal stress
04 Characterise waveform and uncertainty
05 Test commercial high-bandwidth sensors
06 Compare WP4 generators and standards